

TRANSMISSION METHOD AND NETWORK SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates generally to a transmission method and a network system. More particularly, the invention relates to a transmission method and a network system for accommodating a plurality of kinds of traffics (STM, ATM, IP and so forth) in a common network.

10 Description of the Related Art

Conventional network has been constructed with taking a circuit switched network centered at a voice telephone network and private line as a center thereof. However, in the recent years, associating with quick growth of internet, network using an IP (internet protocol) is abruptly growing. Also, in the sound circuit, increase of traffic using modems stresses use condition of circuit switching system.

On the other hand, as modes of circuit switching, there are Synchronous Transfer Mode (STM), Asynchronous Transfer Mode (ATM) and Internet Protocol (IP) establishing respectively independent networks. For example, IP data is transferred to an IP network established by routers and private lines after circuit switching process and ATM network is established as the system considering data transfer. The transmission system is speeded up by Synchronous Optical

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Network/Synchronous Digital Hierarchy SONET/SDH) and is increased a capacity by introduction of Dense Wavelength Division Multiplexing (DWDM)

However, as a result that operation with establishing
5 the independent networks with complicate compromise of various factors, establishment, operation and maintenance of the networks become complicate. Accordingly, for solving such problem, it is inherent to accommodate STM, ATM and IP in a single network.

10 SUMMARY OF THE INVENTION

The present invention has been worked out in order to solve such problems. It is, therefore, an object of the present invention to provide a transmission method and a network system which can accommodate STM, ATM and IP in a single network by
15 newly proposing a frame network to be used in common in physical layer and data link layer.

According to the first aspect of the present invention, a transmission method comprises:

transmitting a plurality of packets in multiplexing
20 manner, which header in each packet includes a first field holding a signal indicative of a packet length, a second field holding a signal indicative of a preferential order upon transferring the packet, a third field holding a signal indicative of a kind of traffic, a fourth field holding a signal
25 indicative of a header length, a fifth field holding a control

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signal depending upon the kind of traffic, and a sixth field holding a signal indicative of a result of CRC operation of the header, a payload holding information signal depending upon kind of the traffic and a signal indicative of a result
5 of CRC operation of the payload.

In the preferred construction, the traffic is one or more kinds among a synchronous transmission mode(STM), asynchronous transmission mode(ATM) and an internet protocol(IP). The payload a may have maximum length and a variable length.

10 The fifth field may be consisted of a field holding a signal indicative of a destination address, a field holding a signal indicative of a sender address, a field holding a remote alarm indicative of an alarm condition in a remote station, and a field holding a remote monitor indicative of a signal
15 receiving condition of the remote station, and the header forms a header of the packet for transmitting a synchronous transmission mode signal.

In the alternative, the fifth field may be consisted of a field holding a signal indicative of a destination address,
20 a field holding a signal indicative of a sender address and a field reserved for future use, and the header is a header of the packet for transmission of an asynchronous transmission mode cell.

In the further alternative, the fifth field may be
25 consisted of a field holding a signal indicative of a label

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and a field reserved for future use, and the header is a header for transmitting the packet according to IPv4 or IPv6 using a label technology.

In a still further alternative, the fifth field may be
5 consisted of a field holding a signal indicative of a
destination address and a field holding a route information
and an identifier for controlling traffic class and flow
spreading, and the header is a header for transmitting the
packet according to IPv4 or IPv6 using an address in the network.

10 In either case, the header may further include a
extendable field by option following the sixth field.

The multiplexed packet may further include an OAM packet used for maintenance of a network and management of operation, and stuff bytes for maintaining a period of the multiplexed packet. The OAM packet may be consisted of a field holding a byte for automatic protection switch, a field holding an order wire, a field of holding a data communication channel, a field holding a remote alarm indicative of alarm condition in the remote station, and a field holding a remote monitor indicative of the signal receiving condition in the remote station.

The stuff byte and the first field holding the signal indicative of the packet length may be converted into a complete representation system with taking a predetermined offset as a law for preventing them from generating continuous "0".

25 According to the second aspect of the present invention,

a network system comprises:

transmitting portion transmitting a plurality of packets with multiplexing, which header in each packet includes a first field holding a signal indicative of a packet length, a second field holding a signal indicative of a preferential order upon 5 transferring the packet, a third field holding a signal indicative of a kind of traffic, a fourth field holding a signal indicative of a header length, a fifth field holding a control signal depending upon the kind of traffic, and a sixth field 10 holding a signal indicative of a result of CRC operation of the header, a payload holding information signal depending upon kind of the traffic and a signal indicative of a result of CRC operation of the payload;

a relay node outputting the packet to an output path 15 depending upon the destination address or a label added to the packet received from the transmitting portion; and

a receiving portion separating the packet received from the relay node and inputting to a switching equipment, an asynchronous transmission mode switch or internet protocol 20 router after performing a predetermined speed changing process.

In the preferred construction, the traffic is one or more kinds among a synchronous transmission mode (STM), asynchronous transmission mode (ATM) and an internet protocol (IP). The 25 payload may have a maximum length and a variable length.

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The fifth field may be consisted of a field holding a signal indicative of a destination address, a field holding a signal indicative of a sender address, a field holding a remote alarm indicative of an alarm condition in a remote station, and a field holding a remote monitor indicative of a signal receiving condition of the remote station, and the header forms a header of the packet for transmitting a synchronous transmission mode signal.

In the alternative, the fifth field may be consisted of a field holding a signal indicative of a destination address, a field holding a signal indicative of a sender address and a field reserved for future use, and the header is a header of the packet for transmission of an asynchronous transmission mode cell.

In the further alternative, the fifth field may be consisted of a field holding a signal indicative of a label and a field reserved for future use, and the header is a header for transmitting the packet according to IPv4 or IPv6 using a label technology.

In a still further alternative, the fifth field may be consisted of a field holding a signal indicative of a destination address and a field holding a route information and an identifier for controlling traffic class and flow spreading, and the header is a header for transmitting the packet according to IPv4 or IPv6 using an address in network.

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In either case, the header may further include a extendable field by option following the sixth field.

The multiplexed packet may further include an OAM packet used for maintenance of a network and management of operation, and stuff bytes for maintaining a period of the multiplexed packet. The OAM packet may be consisted of a field holding a byte for automatic protection switch, a field holding an order wire, a field of holding a data communication channel, a field holding a remote alarm indicative of alarm condition in the remote station, and a field holding a remote monitor indicative of the signal receiving condition in the remote station.

The stuff byte and the first field holding the signal indicative of the packet length may be converted into a complete representation system with taking a predetermined offset as a law for preventing them from generating cintunymous "0".

The multiplexed packet may further include an OAM packet used for maintenance of the network and management of operation, and stuff bytes for maintaining a period of the multiplexed packet.

In the preferred construction, the transmitting portion may comprise:

(a) a switching equipment constituted of a digital subscriber transporting device, a local switching equipment or a tandem switching equipment, a signal processing portion processing a synchronous transmission mode signal output from

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generating portion generating an OAM packet for outputting.

The relay node may comprise a packet synchronization circuit establishing synchronization of the packet using the result of CRC operation of the header included in the packet per input path and the stuff byte, a physical phase/data integrated switch determining an output path of each packet with reference to the destination address or label in the header of the packet, and a packet frame forming portion for re-forming a frame of the packet using the stuff byte. The packet synchronization circuit may use $X^{16} + X^{12} + X^5 + 1$ as generating polygonal expression in the CRC operation of the header. The packet synchronization circuit may establishes synchronization using the stuff byte.

The receiving portion may comprise:

(a) a packet demultiplexing portion separating received packets and an OAM packet detecting portion for detecting the OAM packet;

(b) a first packet decomposing portion processing a signaling packet in synchronous transmission mode input from the packet demultiplexing portion for generating and outputting data, clock and a primitive, a first speed changing portion generating an original clock in the sender on the basis of a received clock, a second packet decomposing portion processing the packet in synchronous transmission mode input from the packet demultiplexing portion for generating and

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(c) a third packet decomposing portion processing a signaling packet in asynchronous transmission mode input from the packet demultiplexing portion for generating and outputting data and clock, a third speed changing portion generating an original clock in the sender on the basis of a received clock, and the asynchronous transmission mode switch receiving an outputs of the third speed changing portion; and

The speed changing portion may comprises a buffer memory storing the clock output from the packet decomposing portion and a PLL extracting an average frequency of the clock before being stored in the buffer memory for reading out the clock stored in the buffer memory according to the clock of the average

frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given herebelow and from the accompanying drawings of the preferred embodiment of the present invention, which, however, should not be taken to be limitative to the invention, but are for explanation and understanding only.

In the drawings:

10 Fig. 1 is an explanatory illustration showing one embodiment of a frame structure (base frame) according to the present invention;

Fig. 2 is an explanatory illustration showing packet arrangement;

15 Fig. 3 is an explanatory illustration showing a header structure in case of STM;

Fig. 4 is an explanatory illustration showing a header structure in case of ATM;

20 Fig. 5 is an explanatory illustration showing a structure of the header in case of IPv4, v6 to be transferred using label technology;

Fig. 6 is an explanatory illustration showing a structure of the header in case of IPv4, v6 transferring using an address in a network;

25 Fig. 7 is an explanatory illustration showing a header

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extension;

Fig. 8 is an explanatory illustration showing a structure of an OAM packet;

Fig. 9 is an explanatory illustration showing a structure
5 of a stuff byte;

Fig. 10 is a block diagram showing a construction of a transmitting portion;

Fig. 11 is a block diagram showing a construction of a relay node;

10 Fig. 12 is a block diagram showing a construction of a relay node;

Fig. 13 is a block diagram showing a construction of a receiving portion; and

15 Fig. 14 is a block diagram showing a construction of a speed changing portion.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention will be discussed hereinafter in detail in terms of the preferred embodiment of the present invention with reference to the accompanying drawings. In the
20 following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to those skilled in the art that the present invention may be practiced without these specific details. In other instance, well-known
25 structures are not shown in detail in order to avoid

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unnecessarily obscure the present invention.

[Frame Structure]

Fig. 1 is an explanatory illustration showing one embodiment of the present invention. As shown in Fig. 1, a basic frame structure is consisted of a header (12 bytes (which can be extended up to 44 bytes as option), a payload (0 to 64 Kbytes) and a result of arithmetic operation of a payload of Cyclic Redundancy Check (CRC) 16 or CRC 32. In the payload portion, voice 64 Kbps x n (STN), a plurality of ATM having the same VPI (Virtual Path Identifier) and IP packet divided per destinations are accommodated as respective independent packets.

Fig. 2 is an explanatory illustration showing a condition where a plurality of packets shown in Fig. 1 are accommodated. The packets are accommodated with taking 125 μ s as one period. In the shown packet arrangement, STM is given the highest preferential order to accommodate. Then, ATM is accommodated as given the second highest preferential order. Then, the IP packet given the lowest preferential order is accommodated in a remaining space. In order to keep 125 μ s or to establish bit synchronization, necessary number of stuff bytes of 2 byte length are added. Furthermore, as used in Wavelength Division Multiplexing (WDM), operation administration and maintenance (OAM) packet is inserted in 125 μ s period as an option. It

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should be noted that, in the drawings, CBR represents a packet accommodating the STM or ATM and IP represents the IP packet.

Next, discussion will be given for a header structure for respective communication mode.

5 Fig. 3 is an explanatory illustration of the header structure in the case of STM. In case of STM, the packet length indicative of entire length of the packet is 2 bytes, a preference indicative of the preferential order of the packet is 1 byte, a high layer protocol as an identifier identifying
10 a signal mounted on the payload is 4 bits, a header length indicative of length of the header is 4 bits, a destination address of the destination is 2 bytes, a sender address is 2 bytes, 1 byte of remote alarm indicative of alarm condition of remote station is added and 2 bytes of header CRC 16
15 transferring result of arithmetic operation by the CRC 16 of the header, finally to form the header. It should be noted that the header length is 0 to F_{hex} (X_{hex} represents that X is a hexa-decimal number) and can be added after CRC 16 up to 32 bytes taking 2 bytes as basic unit.

20 Fig. 4 is an explanatory illustration of the header structure in the case of ATM. In case of ATM, the packet length indicative of entire length of the packet is 2 bytes, a preference indicative of the preferential order of the packet is 1 byte, a high layer protocol as an identifier identifying
25 a signal mounted on the payload is 4 bits, a header length

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indicative of length of the header is 4 bits, a destination address of the destination is 4 bytes, 2 byte of a reserved byte reserved for used in the future is added and 2 bytes of header CRC 16 transferring result of arithmetic operation by the CRC 16 of the header, finally to form the header. It should be noted that the header length is 0 to F_{hex} and can be added after CRC 16 up to 32 bytes taking 2 bytes as basic unit.

Fig. 5 is an explanatory illustration of the header structure in the case of IPv4 and v6 for transferring using a label technology. In case of IPv4, v6 transferring using the label technology, the packet length indicative of entire length of the packet is 2 bytes, a preference indicative of the preferential order of the packet is 1 byte, a high layer protocol as an identifier identifying a signal mounted on the payload is 4 bits, a header length indicative of length of the header is 4 bits, a label for indicating route traffic class as route information of the packet and flow spreading is 4 bytes, 2 byte of a reserved byte reserved for used in the future is added and 2 bytes of header CRC 16 transferring result of arithmetic operation by the CRC 16 of the header, finally to form the header. It should be noted that the header length is 0 to F_{hex} and can be added after CRC 16 up to 32 bytes taking 2 bytes as basic unit. On the other hand, when the traffic to be transferred is IP, lower two bits of the high layer protocol is used. When the packet is constituted over $125 \mu s$, the packet is transferred

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as being divided into arbitrary length of packets.

Fig. 6 is an explanatory illustration showing a header structure of the case of IP4v, 6v transferring using the address in the network. In case of transferring IP4v, 6v using the address in the network, the packet length indicative of entire length of the packet is 2 bytes, a preference indicative of the preferential order of the packet is 1 byte, a high layer protocol as an identifier identifying a signal mounted on the payload is 4 bits, a header length indicative of length of the header is 4 bits, a destination address as recipient address is 4 bytes, 1 byte of identifier for identification of traffic class and flow spreading, and finally, and 2 bytes of header CRC 16 transferring result of arithmetic operation by the CRC 16 of the header, finally to form the header. It should be noted that the header length is 0 to F_{hex} (X_{hex} represents that X is a hexa-decimal number) and can be added after CRC 16 up to 32 bytes taking 2 bytes as basic unit. The extended condition of the header is shown in Fig. 7. When the traffic to be transferred is IP, lower 2bits of the high layer protocol is used. When the packet is constituted over $125 \mu s$, the packet is transferred as being divided into arbitrary length of packets.

Fig. 8 is an explanatory illustration showing a header structure in the case of OAM packet. In the OAM packet to be transferred using the address in the network, the packet of

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packet length C_{hex} is generated per 125 μs . The packet is consisted of K1, K2 bytes for automatic protection switching (APS) and respective bytes of an order wire, DCC (Data Communication Channel: DCC)1, DCC2 and DCC3, remote alarm, remote monitor, and a result of arithmetic operation of CRC16 of header, finally.

Fig. 9 is an illustration showing a stuff byte. As shown in Fig. 9, the stuff byte is a packet of 2 bytes. A code to be added to the packet adds an appropriate offset for 2_{hex} to avoid occurrence of continuous "0". On the other hand, the header length of each packet is adjusted by an offset value. Namely, the stuff byte and the field holding the signal indicative of the packet length are converted into a complete representation system with taking a predetermined offset as a law.

[Network System]

Next, discussion will be given for a transmitting portion, a relay node and a receiving portion forming the shown embodiment of the network system.

Fig. 10 is a block diagram showing the transmitting portion. The transmitting portion 100 has a switching equipment 101, an ATM switch 102, an IP router 103, a signal processing portion 104, an ATM processing portion 105, an ATM cell order control portion 106, an IP preference control portion 107, an FIFO 108, a packet composing portion 109, a

packet multiplexing portion 110, a stuff byte generating portion 111 and an OAM packet generating portion 112.

Fig. 11 is a block diagram showing a relay node. In Fig. 11, the relay node 200 has a physical layer/data link layer integrated switch 201 connected to input lines A and B and output lines A, B and C. The detail of the relay node 200 is as shown in Fig. 12. The relay node 210 includes packet synchronization circuits 211 and 212 for establishing packet synchronization by byte synchronization of arithmetic operation of CRC 16 of the header contained in the data packet of each input line and stuffing byte, the physical layer/data link layer integrated switch 213 determining a route to destination per packet, and packet frame establishing portion 214 to 216 for re-establishing a packet frame by packet stuffing using the packet stuff byte for transferring packet to the output line.

Fig. 13 is a block diagram showing a receiving portion. As shown in Fig. 13, the receiving portion 300 has a packet demultiplexing portion 301, a packet decomposing portion 302 and 303, a speed changing portion 304, a switching equipment 305, an ATM switch 306, an IP router 307 and an OAM packet detecting portion 308.

Fig. 14 is a block diagram showing a construction of the speed changing portion reproducing an original data string. In Fig. 14, the speed changing portion 400 includes a buffer memory 401 and a PLL 402. Accordingly, data extracted by the

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packet decomposing portion 302 is written in the buffer memory 401 by a clock (hereinafter referred to as writing clock) generated by the packet decomposing portion 302. On the other hand, the writing clock is written in the PLL 402 to be extracted
5 an average frequency. By the clock, data is read out from the buffer memory 401 to reproduce the original data string.

A signaling and STM signal reproduced by the speed changing portions (1) and (2) are fed to DLC, LS or TS to be subject to switching process. The ATM cell reproduced by the
10 speed changing portion (3) is transferred to ATM switch to be subject to cell switching process. The IP data reproduced by the speed switching portion (4) is transmitted to the IP router to be subject to a process by the internet protocol.

In the OAM packet detecting portion 308, OAM packet is
15 terminated and K1, K2 byte, order wire, data communication channel and remote alarm and remote monitor are respectively terminated and appropriately processed.

[Operation of Transmitting Portion and Receiving Portion]

Next, discussion will be given for transmitting portion
20 100. In composing of the STM packet, a data string and signal information of 64 kbps x n consisted of 8 bits/125 μ s per one voice channel identified per destination are transmitted to the STM processing portion 105 and the signal processing portion 104. In the STM processing portion 104, leading
25 position and data length of the STM signal aligned per byte

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are identified. The output signal from the STM processing portion 105 is temporarily stored in FIFO (2) per 125 μ s. In the signal processing portion 104, the signaling information per byte of STM are composed into an appropriate length of data string, and the length thereof is measured. The data output from the signal processing portion 104 is temporarily stored in FIFO (1).

In composing of the ATM packet, the ATM cell is input to the ATM cell order control portion 106 from the ATM switch 102, the same VPI packet data per a unit of 125 μ s are rearranged in order measure length of a group of cells having the same VPI. The output of the ATM cell order control portion 106 is temporarily stored in FIFO (3).

In composing of the IP packet, the IP packet data transmitted from the IP router 103 is input to the IP preference control portion 107 for recognizing preference of the IP packet data. The IP packet data of the same destination at the same preference are concentrated, recognized and output in preferential order to be temporarily stored in the FIFO (4). It should be noted that the IP packets as option are composed alone, respectively.

In composing of the packet composing portion (1), respective counterparts to exchanging signaling are added per respective signal information and composed in the header

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composed header, arithmetic operation of CRC 16 is performed with respect to the composed header. Then, the result of the arithmetic operation is added to the tail end of the header. Following the header, data, namely, payload is composed.

5 Furthermore, as an option, the result of arithmetic operation of CRC 16 or CRC 32 is added as option.

In the packet composing portion (3), destination to be exchanged per group of the cells of the same VPI is added per group of the cell to compose in the header together with the

10 own address. In the header, (header length + data length) is composed at the leading end. Then, each packet is formed. In the preference field of the header of the ATM packet, order of the preference is added in order of CBR, then UBR+. As high layer protocol, the identifier of the ATM is added. On the

15 other hand, as the header length in normal case, 0_{hex} is used. On the other hand, the reserved field for use in the future is added. Furthermore, for the composed header, arithmetic operation of CRC 16 is performed with respect to the composed header. Then, the result of the arithmetic operation is added

20 to the tail end of the header. Following the header, data, namely, payload is composed. Furthermore, as an option, the result of arithmetic operation of CRC 16 or CRC 32 is added as option.

In the packet composing portion (4), the route, traffic

25 class and flow spreading information are added as the label

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per each IP data packet. In the header, (header length + data length) is composed at the leading end. Then, each packet is formed. In the preference field of the header of the IP packet, the determined preferential order is added. As high layer
5 protocol, the identifier of the IP is added. On the other hand, as the header length in normal case, 0_{hex} is used. Then, the result of the arithmetic operation is added to the tail end of the header. Following the header, data, namely, payload is composed. Furthermore, as an option, the result of arithmetic
10 operation of CRC 16 or CRC 32 is added as option.

On the other hand, as used in WDM, the OAM packet generating portion is added as an option. In the OAM packet generating portion, the packet having packet length c_{hex} is generated at every $125 \mu\text{s}$. The packet is consisted of
15 respective bytes of K1, K2 bytes for automatic protection switch, order wire, data communication channels DCC1, DCC2 and DCC 3 and remote alarm and remote monitor notifying to the remote station the receiving condition of the OAM packet transmitted from the remote station, and the result pf arithmetic operation
20 of the CRC 16 is added at the tail end of the header.

Furthermore, in the stuff byte generating portion 111, the packet for stuff of 2 byte length is generated. The code to be added to the packet is added an appropriate offset to 2_{hex} for avoiding occurrence of continuous "0". Namely, the
25 stuff byte and the field holding the signal indicative of the

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packet length are converted into a complete representation system with taking a predetermined offset as a law.

Finally, in the packet multiplexing portion 110, the packets which is composed in the packet composing portion with taking the OAM packet at the leading end when the OAM packet is used and with taking the STM packet at the leading end when the OAM packet is not used, are multiplexed. At this time, when empty space is present after multiplexing since bit synchronization is established by only composed packet strings, stuff bytes are filled in the extent of empty space. It should be noted that since the stuff byte is 2 bytes, the leading packet to be a reference of 125 μ s may fluctuate for 2 bytes in the worst case. In the packet multiplexing portion, the multiplexed output is handled as 0ch path of the WDM or the path of the SONET/SDH.

Next, discussion will be given for the operation of the relay node. In the relay node 210, packet synchronization is established by the arithmetic operation of CRC 16 of the header and byte synchronization of the stuffing byte included in the data and packet. Next, by checking the destination address or label field included in the header of the packet, transfer route is determined per packet. Then, the packet is transferred to the output route. At this time, when the STM packet passes, a return path having the same capacity as the selected route is established.

Next, discussion will be given for the receiving portion. In the packet demultiplexing portion 301, bit synchronization and packet synchronization (frame synchronization) is established by the header and the stuffing bytes of each packet.

5 Packet synchronization is judged by a check result of CRC 16 of the header. If the check result of CRC 16 of the header is 0, judgment is made that packet synchronization is established. Depending upon the header length, end of the packet is judged. Subsequently, check of the CRC 16 included in the header of

10 the next packet is performed.

On the other hand, the stuff byte is verified a pattern by a synchronization circuit having a unique pattern for checking synchronization per 2 bytes. Thus, packet synchronization is established. When packet synchronization

15 is established in the packet demultiplexing portion, the high layer protocol in the header is made reference to discriminate data between signaling of STM, STM, ATM or IP.

On the other hand, reference is made to the header length to check whether additional information of the header is

20 present or not. Then, entire packet is comprehended by the packet length and boundary of the payload portion is recognized. In case of the signaling packet of STM, the packet is transferred to the packet decomposing portion (1). In case of the STM packet, the packet is transferred to the packet decomposing

25 portion (2). In case of the ATM packet, the packet is

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transferred to the packet decomposing portion (3). In case of the IP packet, the packet is transferred to the packet decomposing portion (4). On the other hand, in case of the OAM packet, the packet is transferred to the OAN packet
5 detecting portion 308.

In the packet decomposing portion (1), the signaling packet of STM is processed, CRC 16 or CRC 32 of the payload is calculated to generate data, clock and primitive. Data is constituted of a portion where the header and the CRC check
10 byte of the payload are removed. The clock is corresponded in one to one basis to data for taking timing of data. In the primitive, information of sender is included.

In the packet decomposing portion (2), the STM packet is processed, CRC 16 or CRC 32 of the payload is calculated
15 to generate data, clock and primitive. Data is constituted of a portion where the header and the CRC check byte of the payload are removed. The clock is corresponded in one to one basis to data for taking timing of data. In the primitive, information of sender is included.

In the packet decomposing portion (3), the ATM packet is processed, CRC 16 or CRC 32 of the payload is calculated
20 to generate data and clock. Data is constituted of a portion where the header and the CRC check byte of the payload are removed. The clock is corresponded in one to one basis to data
25 for taking timing of data.

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In the packet decomposing portion (4), the IP packet is processed, CRC 16 or CRC 32 of the payload is calculated to generate data and clock. Data is constituted of a portion where the header and the CRC check byte of the payload are removed.

5 The clock is corresponded in one to one basis to data for taking timing of data.

Next, in the speed changing portion (1), the original signal of the sender is reproduced by smoothing the clock by PLL or the like.

10 In the speed changing portion (2), the original signal of the sender is reproduced by smoothing the clock by PLL or the like.

In the speed changing portion (3), the original signal of the sender is reproduced by smoothing the clock by PLL or
15 the like.

In the speed changing portion (4), the original signal of the sender is reproduced by smoothing the clock by PLL or the like. The basic construction of the speed changing portion is constructed with the buffer memory. The data extracted by
20 the packet decomposing portion is written in the buffer memory
40 by the clock (hereinafter referred to as writing clock) generated by the packet decomposing portion 302. On the other hand, the writing clock is written in PLL 402 to be extracted an average frequency. By reading out data from the buffer
25 memory by the clock, the original data string is reproduced.

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Next, discussion will be given for arithmetic operation of CRC 16 of the header. Generated polygonal expression of CRC 16 is $X^{16} + X^{12} + X^5 + 1$. Data to be object for arithmetic operation of CRC becomes $8 \times 10 = 80$ bits. Here, considering a unit matrix of 80 rows x 80 columns, X^{16} is multiplied per row and is subtracted from the generated polygonal expression to derive a remainder. The remainder, namely transposed matrix of a matrix of 80 rows x 16 columns is taken, the resultant value is expressed as [P]. To this transposed matrix, a column vector [A] consisted objection is multiplied. At this time, in calculation of sum of products of this matrix, mod2 operation is performed to derive the result of arithmetic operation of CRC 16. This value is added as header CRC 16.

In the packet synchronization circuits 211 and 212, for the foregoing transposed matrix [P], [PI] matrix is generated with taking 16 rows x 16 columns as unit matrix. To this matrix, a column vector [B] consisted of header 96 code is multiplied. At this time, in operation of sum of products of the matrix. mod2 operation is performed. Then, when all result become 0, judgment is made that the header is detected, and count is performed for the packet length indicated by the most significant 16 bits. Then, CRC operation is performed in similar manner as the next header. When synchronization is not established, memory of 96 bits is prepared for performing the foregoing operation per 1 bit shift to continue shifting until

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As set forth above, the present invention comprises transmitting a plurality of packets in multiplexing manner, which header in each packet includes a first field holding a signal indicative of a packet length, a second field holding a signal indicative of a preferential order upon transferring the packet, a third field holding a signal indicative of a kind of traffic, a fourth field holding a signal indicative of a header length, a fifth field holding a control signal depending upon the kind of traffic, and a sixth field holding a signal indicative of a result of CRC operation of the header, a payload holding information signal depending upon kind of the traffic and a signal indicative of a result of CRC operation of the payload.

Accordingly, by inserting the stuff byte using the frame
25 structure integrated therein the physical layer and the data

Although the present invention has been illustrated and described with respect to exemplary embodiment thereof, it should be understood by those skilled in the art that the foregoing and various other changes, omissions and additions may be made therein and thereto, without departing from the spirit and scope of the present invention. Therefore, the present invention should not be understood as limited to the specific embodiment set out above but to include all possible embodiments which can be embodied within a scope encompassed

and equivalents thereof with respect to the feature set out
in the appended claims.

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